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polysilicon region doped with an N type impurity and a P+ polysilicon region doped with a P type impurity. The present inventors have recognized that many P+ and N+ dopant materials are subject to migration from a given polysilicon layer to another polysilicon layer, to an overlying conductive layer, or to another region of the given polysilicon layer. As a result, these opposite types of impurities are subject to cross diffusion. This cross diffusion can lead to performance degradation in the integrated circuit device.--

Please replace the following paragraphs starting after the "BRIEF SUMMARY OF THE INVENTION" and ending on page 6, line 24, with:

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--This need is met by the present invention wherein an ultrathin buried diffusion barrier layer (UBDBL) is formed over all or part of the doped polysilicon layer of a polysilicide structure composed of the polycrystalline silicon film and an overlying film of a metal, metal silicide, or metal nitride.

In accordance with one embodiment of the present invention, a memory cell is provided comprising a semiconductor substrate, a P well, an N well, an N type active region, a P type active region, an isolation region, a polysilicide gate electrode structure, and a diffusion barrier layer. The P well is formed in the semiconductor substrate. The N well is formed in the semiconductor substrate adjacent to the P well. The N type active region is defined in the P well and the P type active region is defined in the N well. The isolation region is arranged to isolate the N type active region from the P type active region. The polysilicide gate electrode structure is composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film. The polycrystalline silicon film comprises an N+ polysilicon layer over the N type active region and a P+ polysilicon layer over the P type active region. The diffusion barrier layer is formed in the polysilicide gate electrode structure over a substantial portion of the polycrystalline silicon film between the polycrystalline silicon film and the metal, metal silicide, or metal nitride film.

In accordance with another embodiment of the present invention, a memory cell is provide comprising a semiconductor substrate, a P well, an N well, an NMOS transistor, a PMOS transistor, an isolation region, a polysilicide gate electrode structure, and a diffusion barrier layer. The P well is formed in the semiconductor substrate. The N well is formed in the

semiconductor substrate. The NMOS transistor defines an N type active region in the P well. The PMOS transistor defining a P type active region in the N well. The isolation region is arranged to isolate the N type active region from the P type active region. The polysilicide gate electrode structure is composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film. The polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of the NMOS transistor and a P+ polysilicon layer forming a portion of the PMOS transistor. The diffusion barrier layer is formed in the polysilicide gate electrode structure over a substantial portion of the polycrystalline silicon film between the polycrystalline silicon film and the metal, metal silicide, or metal nitride film.

Preferably, the diffusion barrier layer comprises an ultrathin diffusion barrier layer and has a thickness of between about 5 Å and about 25 Å.

In accordance with yet another embodiment of the present invention, an SRAM memory cell is provided comprising a semiconductor substrate, a P well, an N well, a flip flop, an isolation region, a polysilicide gate electrode structure, and a diffusion barrier layer. The P well formed in the semiconductor substrate. The N well formed is in the semiconductor substrate. The flip-flop is formed by two access transistors and a pair of cross coupled inverters. Each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor. The pull-up transistor defines a P type active region in the N well and the pull-down transistor defines an N type active region in the P well. The isolation region is arranged to isolate the N type active region from the P type active region. The polysilicide gate electrode structure is composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film. The polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of the pull-down transistor and a P+ polysilicon layer forming a portion of the pull-up transistor. The diffusion barrier layer is formed in the polysilicide gate electrode structure between the polycrystalline silicon film and the metal, metal silicide, or metal nitride film over a substantial portion of the polycrystalline silicon film.

In accordance with yet another embodiment of the present invention, an SRAM memory cell is provided comprising a semiconductor substrate, a P well, an N well, a flip flop, an isolation region, a polysilicide gate electrode structure, and a diffusion barrier layer. The flip-flop is formed by two access transistors and a pair of cross coupled inverters. Each pair of cross-

coupled inverters includes a pull up transistor and a pull down transistor. The pull-up transistor defines a P type active region in the N well and the pull-down transistor defines an N type active region in the P well. The isolation region is arranged to isolate the N type active region from the P type active region. The polysilicide gate electrode structure is composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film. The polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of the pull-down transistor and a P+ polysilicon layer forming a portion of the pull-up transistor. The diffusion barrier layer is formed in the polysilicide gate electrode structure between the polycrystalline silicon film and the metal, metal silicide, or metal nitride film over a substantial portion of the N+ polysilicon layer and the P+ polysilicon layer.

In accordance with yet another embodiment of the present invention, a memory cell array is provided comprising a plurality of SRAM cells arranged in rows and columns. Each cell of the array is connected to a word line and to a pair of bit lines and comprises a semiconductor substrate, a P well, an N well, a flip flop, an isolation region, a polysilicide gate electrode structure, and a diffusion barrier layer. The flip-flop is formed by two access transistors and a pair of cross coupled inverters. Each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor. The pull-up transistor defines a P type active region in the N well and the pull-down transistor defines an N type active region in the P well. The isolation region is arranged to isolate the N type active region from the P type active region. The polysilicide gate electrode structure is composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film. The polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of the pull-down transistor and a P+ polysilicon layer forming a portion of the pull-up transistor. The diffusion barrier layer is formed in the polysilicide gate electrode structure between the polycrystalline silicon film and the metal, metal silicide, or metal nitride film over a substantial portion of the polycrystalline silicon film.

In accordance with yet another embodiment of the present invention, a computer system is provided including a microprocessor in communication with a memory cell array via a data communication path. The memory cell array comprises a plurality of SRAM cells arranged in rows and columns. Each cell of the array is connected to a word line and to a pair of bit lines and comprises a semiconductor substrate, a P well, an N well, a flip flop, an isolation region, a

polysilicide gate electrode structure, and a diffusion barrier layer. The flip-flop is formed by two access transistors and a pair of cross coupled inverters. Each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor. The pull-up transistor defines a P type active region in the N well and the pull-down transistor defines an N type active region in the P well. An isolation region is arranged to isolate the N type active region from the P type active region. A polysilicide gate electrode structure is composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film. The polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of the pull-down transistor and a P+ polysilicon layer forming a portion of the pull-up transistor. The diffusion barrier layer is formed in the polysilicide gate electrode structure between the polycrystalline silicon film and the metal, metal silicide, or metal nitride film over a substantial portion of the polycrystalline silicon film.

In accordance with yet another embodiment of the present invention, a method of fabricating an SRAM memory cell is provided. Recited in terms of physical location, as opposed to chronological order of processing, the method comprises the steps of (i) providing a semiconductor substrate, (ii) forming a P well in the semiconductor substrate, (iii) forming an N well in the semiconductor substrate, (iv) forming a P type active region of a pull-up transistor in the N well, (v) forming a gate oxide layer and a conductive gate of the pull-up transistor over the P type active region, (vi) forming an N type active region of a pull-down transistor in the P well; (vii) forming a gate oxide layer and a conductive gate of the pull-down transistor over the N type active region, (viii) forming an isolation region between the N type active region and the P type active region, (ix) forming a polycrystalline silicon film over the pull-down transistor and the pull-up transistor, (x) doping selectively the polycrystalline silicon film to form an N+ polysilicon layer over the pull-down transistor and a P+ polysilicon layer over the pull-up transistor; (xi) forming a diffusion barrier layer over a substantial portion of the polycrystalline silicon film, and (xii) forming a metal, metal silicide, or metal nitride film over the doped polycrystalline silicon film and the diffusion barrier layer. The diffusion barrier layer is formed by selective chemical oxidation of the polycrystalline silicon film.

In accordance with yet another embodiment of the present invention, a method of fabricating a memory cell array by arranging a plurality of the SRAM cells in rows and columns

and connecting each SRAM cell of the array to a word line and to a pair of bit lines is provided. Recited in terms of physical location, as opposed to chronological order of processing, each of the SRAM cells is fabricated by (i) providing a semiconductor substrate, (ii) forming a P well in the semiconductor substrate, (iii) forming an N well in the semiconductor substrate, (iv) providing a flip-flop including two access transistors and a pair of cross coupled inverters wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor and wherein the pull-up transistor defines a P type active region in the N well and the pull-down transistor defines an N type active region in the P well, (v) arranging an isolation region to isolate the N type active region from the P type active region, (vi) providing a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein the polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of the pull-down transistor and a P+ polysilicon layer forming a portion of the pull-up transistor, and (vii) forming a diffusion barrier layer in the polysilicide gate electrode structure between the polycrystalline silicon film and the metal, metal silicide, or metal nitride film over a substantial portion of the polycrystalline silicon film.

In accordance with yet another embodiment of the present invention, a method of fabricating a computer system is provided. The computer system is fabricated by arranging a microprocessor in communication with a memory cell array via a data communication path and fabricating the memory cell array by arranging a plurality of the SRAM cells in rows and columns and connecting each SRAM cell of the array to a word line and to a pair of bit lines. Recited in terms of physical location, as opposed to chronological order of processing, each of the SRAM cells is fabricated by (i) providing a semiconductor substrate, (ii) forming a P well in the semiconductor substrate, (iii) forming an N well in the semiconductor substrate, (iv) providing a flip-flop including two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein the pull-up transistor defines a P type active region in the N well and the pull-down transistor defines an N type active region in the P well, (v) arranging an isolation region to isolate the N type active region from the P type active region, (vi) providing a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein the polycrystalline silicon film comprises an

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N+ polysilicon layer forming a portion of the pull-down transistor and a P+ polysilicon layer forming a portion of the pull-up transistor, (vii) forming a diffusion barrier layer in the polysilicide gate electrode structure between the polycrystalline silicon film and the metal, metal silicide, or metal nitride film over a substantial portion of the polycrystalline silicon film.--

Please replace the first paragraph on page 9, with:

A3

--The gate electrode structure of the CMOS structure **4** is constructed to have a laminar or polysilicide structure composed of a polycrystalline silicon film and an overlying film of a metal, metal silicide, or metal nitride. Specifically, the polycrystalline silicon film comprises an N+ polysilicon layer **21** formed over the NMOS transistor **11** and a P+ polysilicon layer **22** formed over the PMOS transistor **12**. Each of the polysilicon layers **21**, **22** typically provide a connection to a transistor gate. The N+ polysilicon layer **21** is doped with an N type impurity such as arsenic (As) or phosphorous P31. The P+ polysilicon layer **22** is doped with an N type impurity such as boron (B). The overlying metal, metal silicide, or metal nitride layer **24** is typically formed of a tungsten silicide (WSi_X: x=**2**, for example) and contributes to an accelerated signal transmission rate because the specific resistance of the metal, metal silicide, or metal nitride layer **24** is lower than that of the polycrystalline silicon layers **21**, **22**. The metal, metal silicide, or metal nitride layer **24** may be made of not only WSi_X but also molybdenum silicide $MoSi_X$, titanium silicide $TiSi_X$, tantalum silicide $TaSi_X$, cobalt silicide, nitrides of these metals, etc. An insulating capping layer **26** is formed over the WSi_X layer **24** and is typically formed of silicon dioxide or silicon nitride.--

Please replace the third paragraph on page 11, starting at line 21 15, with:

A4

--In the embodiment illustrated in Fig. 5, the UBDBL **28** and the polysilicide gate electrode structure are arranged such that the UBDBL **28** is formed over a substantial portion of the P+ polysilicon layer **22** between the P+ polysilicon layer **22** and the metal, metal silicide, or metal nitride film **24** and does not extend over a substantial portion of the N+ polysilicon layer **21**. Stated differently, the UBDBL **28** is arranged such that the

metal, metal silicide, or metal nitride film **24** is in direct contact with the N+ polysilicon layer **21** and defines an N type common boundary with the N+ polysilicon layer **21** that is significantly larger than any P type common boundary defined by the metal, metal silicide, or metal nitride film **24** and the P+ polysilicon layer **22**. The UBDBL **28** may be formed over the entire extent of that portion of the P+ polysilicon layer **22** that is overcoated by the metal, metal silicide, or metal nitride film **24**. In this manner, migration of P+ dopants from the P+ polysilicon layer **22** to the overlying metal, metal silicide, or metal nitride film **24** is significantly impeded by the UBDBL **28**. Although dopants from the N+ polysilicon layer **21** enter the overlying metal, metal silicide, or metal nitride film **24**, cross diffusion and P+ poly gate depletion are suppressed because these dopants, present in the overlying metal, metal silicide, or metal nitride film **24**, cannot cross the UBDBL **28** and enter the P+ polysilicon layer **22**.--

Please replace the paragraphs on page 12, starting at line 9, with:

--Similarly, in the embodiment illustrated in Fig. 6, the UBDBL **28** and the polysilicide gate electrode structure are arranged such that the UBDBL **28** is formed over a substantial portion of the N+ polysilicon layer **21** between the N+ polysilicon layer **21** and the metal, metal silicide, or metal nitride film **24** and does not extend over a substantial portion of the P+ polysilicon layer **22**. Stated differently, the UBDBL **28** is arranged such that the metal, metal silicide, or metal nitride film **24** is in direct contact with the P+ polysilicon layer **22** and defines an P type common boundary with the P+ polysilicon layer **22** that is significantly larger than any N type common boundary defined by the metal, metal silicide, or metal nitride film **24** and the N+ polysilicon layer **21**. The UBDBL **28** may be formed over the entire extent of that portion of the N+ polysilicon layer **21** that is overcoated by the metal, metal silicide, or metal nitride film **24**. In this manner, migration of N+ dopants from the N+ polysilicon layer **21** to the overlying metal, metal silicide, or metal nitride film **26** is significantly impeded by the UBDBL **28**. Although dopants from the P+ polysilicon layer **22** enter the overlying metal, metal silicide, or metal nitride film **24**, cross diffusion and N+ poly gate depletion